EAST Search History

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S2	20	("5055778"|"5289631"|"5513430"|"5604446"|"5625298"|"5642056"|"5804983"|"5808474"|"5828225"|"6075373"|"6292007"|"6359456"|"6426636"|"6426637"|"6426639"|"6551844"|"6552555"|"6597187"|"6621260"|"6621710").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2006/08/03 14:27
S3	96	S1 not S2	US-PGPUB; USPAT; USOCR	OR	ON	2006/08/03 14:27
S4	1	"20040217769"	US-PGPUB; USPAT	OR	OFF	2006/11/17 16:00

EAST Search History

S5	11	(US-20040217769-$).did. or (US-4585991-$ or US-5693565-$ or US-6336269-$ or US-6426638-$ or US-6617865-$ or US-6114864-$ or US-6771084-$ or US-6551844-$ or US-6359456-$ or US-6597187-$). did.	US-PGPUB; USPAT	OR	OFF	2006/11/17 15:39
S6	0	(((die near2 probe) near2 bump) and (thermal or heat$4) same (exapan$4 or contact$4)).clm.	US-PGPUB; USPAT	OR	OFF	2006/11/17 13:23
S7	0	(((die near2 probe) near2 bump) and (thermal or heat$4) same (expan$4 or contact$4)).clm.	US-PGPUB; USPAT	OR	OFF	2006/11/17 13:24
S8	0	(((die near2 probe) near2 bump) and (thermal or heat$4) same (expan$4 or contact$4))	US-PGPUB; USPAT	OR	OFF	2006/11/17 13:24
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S10	1234	((bump) and (thermal or heat$4) same (expan$4 or contact$4)).clm.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/17 13:25
S11	418	((bump) and (thermal or heat$4) same (expan$4 or contact$4)).ab.	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/17 13:25
S12	2	"20040217767"	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/17 15:36
S13	1	"6984996"	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/17 15:04
S14	102	("5066357").PN. OR ("5225037"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/17 15:11
S15	59	S14 and (test$4 near (die or chip))	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/17 15:12
S16	65	S14 and (test$4 near (die or chip))	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/17 15:12
S17	6	S16 not S15	US-PGPUB; USPAT; USOCR	OR	ON	2006/11/17 15:12

EAST Search History

S18	11	(US-20040217769-$).did. or (US-4585991-$ or US-5693565-$ or US-6336269-$ or US-6426638-$ or US-6617865-$ or US-6114864-$ or US-6771084-$ or US-6551844-$ or US-6359456-$ or US-6597187-$). did.	US-PGPUB; USPAT	OR	OFF	2006/11/17 15:39
S19	13	("5055778" | "5513430" | "5604446" | "5642056" | "5804983" | "5828225" | "6075373" | "6359456" | "6426636" | "6426637" | "6426639" | "6552555" | "6621710").PN. OR ("6984996"). URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/17 15:43
S20	3	((probe adj card) and (same$ adj material)).ab.	US-PGPUB; USPAT	OR	OFF	2006/11/17 16:01
S21	18	("5521523" | "5604446" | "5804983" | "5831441" | "6005401" | "6040700" | "6060892" | "6084215" | "6107813" | "6215321" | "6246251" | "6265888").PN. OR ("6480012").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/17 16:08
S22	84	"5625298"	USPAT	OR	OFF	2006/11/17 17:13
S23	19	"5808474"	USPAT	OR	OFF	2006/11/17 17:13
S24	8	"6292007"	USPAT	OR	OFF	2006/11/17 17:13
S25	16	("5268571" | "5475318" | "5623214" | "5642054" | "5773780" | "5806181" | "5829128" | "6060891" | "6072321" | "6100708" | "6143616" | "6181144" | "6187677" | "6379982" | "6531327").PN. OR ("6912778").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/11/17 17:53
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S27	13	(diorio near mark)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2007/11/19 11:40
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EAST Search History

S29	3532	324/754.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 12:12
S30	999	324/755.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 12:12
S31	952	324/758.ccls.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 12:12
S32	53	S29 and S30 and S31	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 12:40
S33	2534	(die or chip) near probe	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 12:26
S34	2229	((die or chip) near probe) and (test$4 or inspect$4)	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 12:27
S35	730	((die or chip) near probe) with (test$4 or inspect$4)	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 12:28
S36	67	(((die or chip) near probe) with (test$4 or inspect$4)).ab.	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 12:35
S37	1117	(wafer near prober)	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 12:36
S38	45	(wafer near prober).ti.	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 12:36
S39	32	(wafer near prober).ti. and (die or chip)	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 13:14
S40	271	S29 and S30	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 13:29
S41	71	(probe adj2 comprising) near2 (die or chip)	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 12:47
S42	14	("5061033" | "5477160" | "5807767" | "6064213" | "6084215" | "6400173" | "6452411" | "6483330" | "6527563" | "6531335" | "6551844" | "6559666").PN. OR ("6847218").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 13:01
S43	4719	test adj (die or chip)	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 13:21

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S44	511	S43 and 324/754-758.ccls.	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 13:15
S45	12	test adj (die or chip) adj (hold$3 or support$4)	US-PGPUB; USPAT; USOCR	OR	ON	2007/11/19 13:21
S50	81	("3473124" | "4061969" | "4244048" | "4344033" | "4772846" | "4777716" | "4780086" | "4801871" | "4937203" | "4975079" | "5012187" | "5128008" | "5134638" | "5148103" | "5172050" | "5173904" | "5210485" | "5224265" | "5228502" | "5241266" | "5279975" | "5307010").PN. OR ("5600257").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 14:20
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S52	24	S50 and wafer and (probe adj card)	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/19 14:20
S59	7447	(plasma with chamber).clm.	USPAT	OR	OFF	2007/11/19 18:29
S60	4140	(plasma with chamber).ab.	USPAT	OR	OFF	2007/11/19 18:29
S61	237	(plasma with chamber).ti.	USPAT	OR	OFF	2007/11/19 18:29
S62	178	S59 and S60 and S61	USPAT	OR	OFF	2007/11/19 18:33
S63	23	("5055778"|"5289631"|"5513430"|"5604446"|"5625298"|"5642056"|"5804983"|"5808474"|"5828225"|"6075373"|"6292007"|"6359456"|"6379982"|"6426636"|"6426637"|"6426639"|"6480012"|"6551844"|"6552555"|"6597187"|"6621260"|"6621710"|"7112975").PN.	USPAT	OR	OFF	2007/11/20 10:54
S64	3	(ceramic with probe with card).ti.	USPAT	OR	OFF	2007/11/20 12:03
S65	10	(ceramic with probe with card).ab.	USPAT	OR	OFF	2007/11/20 12:07
S66	48	((semiconductor or silicon) with probe with card).ti.	USPAT	OR	OFF	2007/11/20 12:08
S67	18	((semiconductor or silicon) near2 (probe adj card)).ti.	USPAT	OR	OFF	2007/11/20 12:23
S68	9	(semiconductor with (chip or die) with probe).ti.	USPAT	OR	OFF	2007/11/20 12:23

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S69	18	("5521523" | "5604446" | "5804983" | "5831441" | "6005401" | "6040700" | "6060892" | "6084215" | "6107813" | "6215321" | "6246251" | "6265888").PN. OR ("6480012").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/20 13:16
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S71	5	(("5159750") or ("5008734") or ("7144759") or ("6975127") or ("6984996")).PN.	USPAT; USOCR	OR	OFF	2007/11/20 13:17

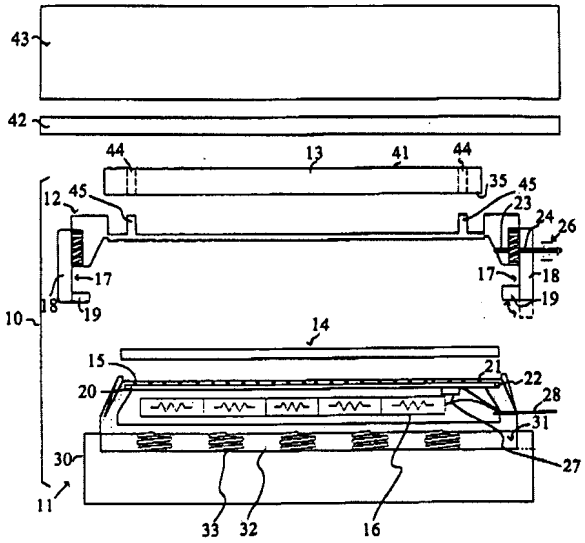

FIG. 1a

probe tips (not shown) of the probe card 13 to enable electrical contact therebetween. In the embodiment of FIG. 1, the elastic member 33 is a spring, biased upwardly. In certain embodiments, a plurality of elastic elements are disposed within the gap, for example, the plurality of springs shown in FIG. 1. The relative resilience of the elastic member also inhibits excess pressure on the substrate contacts and the probe tips of the probe card when the two support members are engaged.

(8) Details of an embodiment of a probe card 13 for electrically interfacing a plurality of contact pads on a substrate to a testing unit are shown in FIGS. 2a, 2b and 3. FIG. 3 is a lateral section of a detail of an embodiment of the probe card of FIG. 2a through section line 3--3, shown aligned above a section of a substrate 14 showing a plurality of probe tips 34 on a surface 35 of the probe card that faces the substrate 14. The probe tips 34 are arranged in a manner corresponding to a plurality of contact pads 36 on the devices of the substrate 14 so that when the probe tip surface 35 of the probe card 13 faces the contact pad surface 37 of the substrate 14 in proper alignment, each probe tip will electrically contact a contact pad. FIG. 3 also shows a plurality of signal contacts 38 on the probe card 13 for conducting signals to and from a testing unit (not shown). Each signal contact is electrically connected to a probe tip. In a preferred embodiment, as shown in FIG. 3, each probe tip 34 extends beyond the surface 35 of the probe card and the probe conductive path 39 between a given signal contact and its corresponding probe tip is shortened to the greatest extent possible to reduce the impedance mismatch problems previously discussed that are exacerbated as the probe wire lengthens. In a preferred embodiment, each signal contact 38 is electrically associated with a ground plane 40 to minimize interference among individual signals.

(9) FIG. 2a is a top elevation of the embodiment of the probe card just described in FIG. 3, showing a plurality of signal contacts 38. FIG. 2b is a bottom view of the embodiment of the probe card of FIG. 3, showing a plurality of probe tips 34. Some of the more numerous signal contacts 38 may be connected to more than one probe tip 34. This may allow different tests to be performed without repositioning the probe card or may allow the probe card to be used with multiple testers. It should be appreciated that different circuits, for example having different loads or impedance matching characteristics, might be included in the different connection paths provided by the embodiments of FIGS. 2a and 2b. The probe card 13 and certain of its elements, for instance the signal contacts 38 and any circuits can be manufactured using standard printed circuit board ("PCB") technology. In one embodiment, the signal contacts 38 and circuits (not shown) are made from boron tungsten. In another embodiment, they are made from copper. Other conductive materials having good electrical properties might also be used. The probe tips 34 can be manufactured using standard

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US006040700A

United States Patent [19]

Berar

[11] **Patent Number: 6,040,700**

[45] **Date of Patent: Mar. 21, 2000**

[54] **SEMICONDUCTOR TESTER SYSTEM INCLUDING TEST HEAD SUPPORTED BY WAFER PROBER FRAME**

[75] Inventor: **Andrei Berar**, Campbell, Calif.

[73] Assignee: **Credence Systems Corporation**, Fremont, Calif.

[21] Appl. No.: 08/929,502

[22] Filed: Sep. 15, 1997

[51] Int. Cl.[7] G01R 31/02

[52] U.S. Cl. 324/754; 324/758

[58] Field of Search 324/754, 758, 324/761, 762, 755, 756, 757, 765

[56] References Cited

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5,804,983 9/1998 Nakajima et al. 324/754

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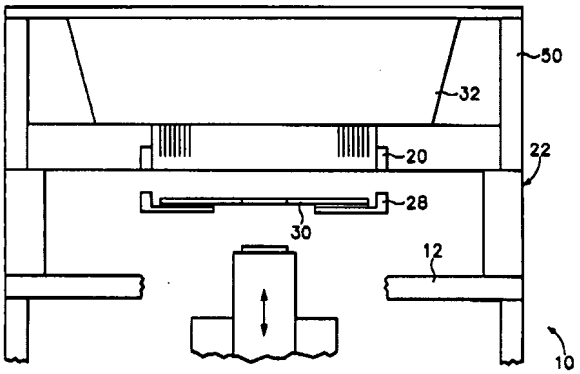
Primary Examiner—Jay Patidar

Attorney, Agent, or Firm—Smith-Hill and Bedell

[57] **ABSTRACT**

In a semiconductor tester system including a wafer prober, the entire weight of the test head assembly is carried by the wafer prober frame. In one embodiment, a probe card is releasably attached to the test head assembly through a ring carrier and the probe tips are planarized during initial installation. In another embodiment, the probe card is attached directly to the test head assembly and the probe tips are planarized each time the probe card is changed.

14 Claims, 2 Drawing Sheets



test head assembly is in contact with the ring carrier 18 and is latched thereto. The test head assembly typically has a mass of at least 150 kg. Most of the weight of the test head assembly is carried by a manipulator 34, but a significant part of the weight of the test head assembly is carried by the ring carrier 18.

(6) When the latch elements 28 of the probe card stiffener 26 are engaged with the latching mechanism 20, the contact pads of the probe card engage spring-loaded contact elements 36 which project downward from the test head assembly and provide electrical connection between the test head assembly and contact pads of the probe card.

(7) For testing an integrated circuit device in wafer form, the wafer 40 is placed on the vacuum chuck 14 and is held in place by partial vacuum applied to the lower surface of the wafer. The vacuum chuck may be moved horizontally to position the contact pads of the wafer vertically below the probe tips and then moves upward and delivers the wafer to a test station in which the contact pads of the wafer engage the probe tips, for making electrical contact with the integrated circuit device, and stimulus and response signals are communicated between the test head and the wafer by way of the contact elements 36 and the conductive traces of the probe card.

(8) It is important that the plane of the contact pads of the wafer 40 be parallel with the plane of the probe tips of the probe card 30 to ensure that the probe tips enter electrically conductive contact with all the pads of the wafer under test when the vacuum chuck is displaced to the test station. For this purpose, at least two of the support points of the ring carrier support structure 22 are individually adjustable in height for adjusting the orientation of the ring carrier 18 relative to the prober frame 12.

(9) Because the weight of the test head assembly 32 is shared between the ring carrier 18 and the manipulator 34, vibration of the floor on which the prober frame and manipulator rest can lead to independent vibration of the test head assembly and ring carrier. Since the test head assembly is latched to the ring carrier, this independent vibration can cause distortion of the ring carrier. Further, the horizontal relative movement of the probe card and the wafer can lead to misalignment of the probe tips with respect to the pads of the device under test, impairing the accuracy of the test to a significant extent, and to erosion of the probe tips, reducing the useful life of the probe card. Moreover, the manipulator includes moving parts which shed debris, which is undesirable in a clean room environment.

(10) SUMMARY OF THE INVENTION

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wafer holder 219/444
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t head
wafer package. 324/754

FIG. 2

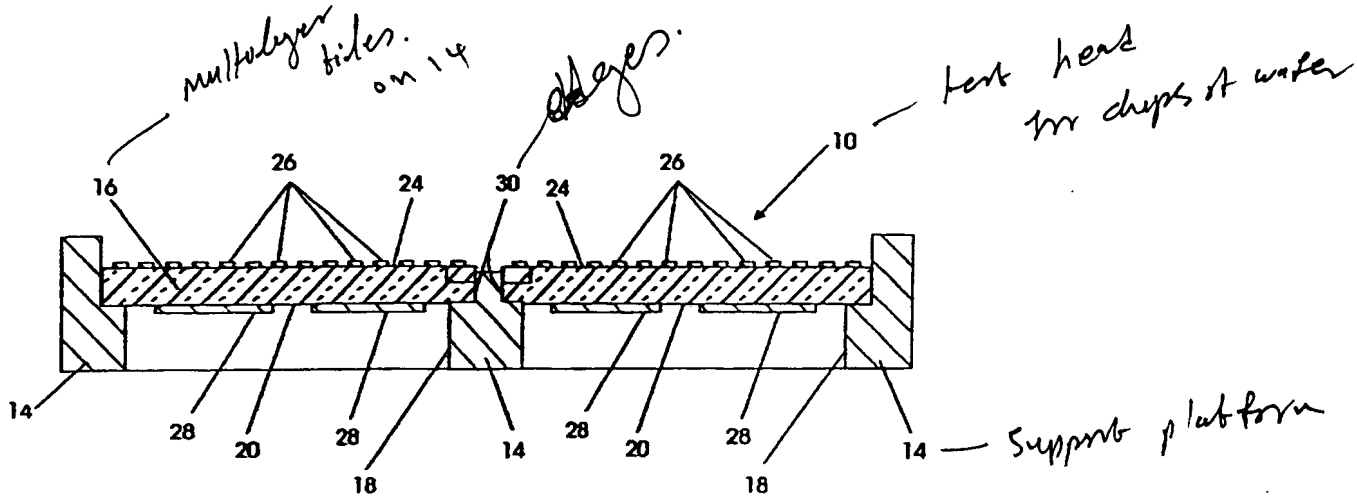
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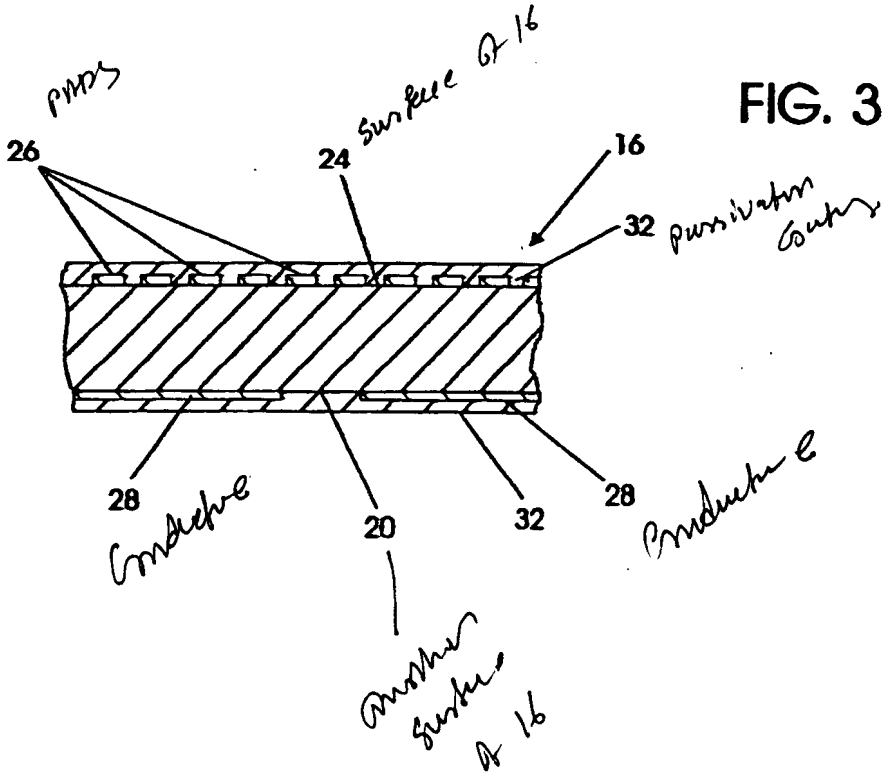
FIG. 3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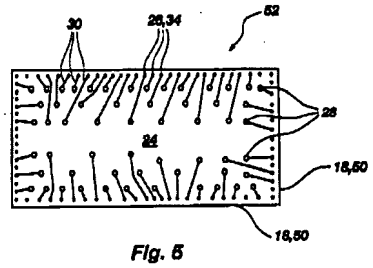

Fig. 5

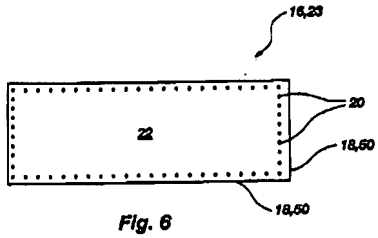

Fig. 6

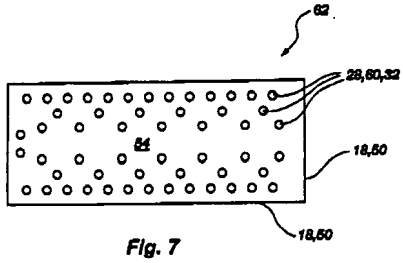

Fig. 7

electrically conductive globules, solder balls, or bumps 32 as described earlier.

(27) The lower most portion of drawing FIG. 11 shows such a representative test probe 46 extending from a isolated portion of probe card 42 and wherein test probe 46 and preferred globule, solder ball, or bump 32 will be brought into contact with each other so as to complete an electrical circuit between test probe 46 which, in turn, is electrically connected by way of test circuit trace, or lead, 56 with burn-in and testing circuit software and hardware (not shown). Because each die bond pad 20 by way of respectively associated globules, solder balls, or bumps 34, conductive traces 30, and conductive filling material 36 allows each die 16 on device wafer 4 to be fully exercised and tested at elevated temperatures and voltages, it is possible to determine and identify which dies are good (KGDs) and which are bad before they are singulated from the wafer-on-wafer package 2. It should be noted that because nonactive surface 6 of device wafer 4 remains exposed and readily accessible, nonactive surface 6 can be provided with, on a temporary or permanent basis, any suitable means for cooling, such as cooling fins, liquid cooling channels, or heat sinks, which can be used to thermally modulate and prevent the overheating of wafer-on-wafer package 2 during burn-in and testing.

(28) Upon wafer-on-wafer package 2 being burned-in and tested, wafer-on-wafer package 2 is removed from burn-in and test apparatus 66 and individual die packages 68 (not shown) are singulated from wafer-on-wafer package 2 along scribe lines 18, which is frequently performed by a high-precision diamond saw. The now singulated individual die packages 68 can then be mounted on the next level of assembly preferably by conventional C4 solderball, or bump, bonding techniques and processes. An isolated portion of a representative singulated individual die package 68 being mounted on a printed circuit board, memory module board, or other suitable mounting substrate 44 is shown in drawing FIG. 12. Singulated individual die package 68 comprises at least one semiconductor die 16 that has been segmented from wafer-on-wafer package 2 (not shown) and thus will comprise a segment of device wafer 4 being respectively connected to a same-sized segment of support wafer 10 generally defined by boundary 50 (not shown in drawing FIG. 12) of die connect region 24. In a similar fashion in which globule, solder ball, or bump 34 is preferably bonded to die bond pad 20, preferred globules, solder balls, or bumps 32 are electrically and mechanically attached to an electrically conductive mounting pad 48 by conventional C4 technology or by other known solder ball, or bump, bonding techniques utilizing elevated temperatures and pressures which are sufficient to reflow and reform globule, solder ball, or bump 32 with mounting pad 48. Mounting pad 48 is usually but one of a plurality of mounting pads 48 positioned on mounting substrate 44 so that

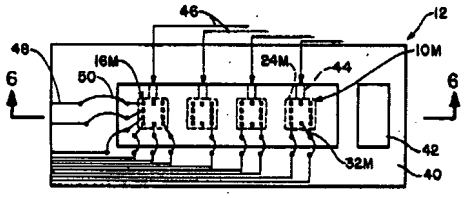

FIGURE 5

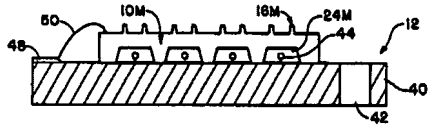

FIGURE 6

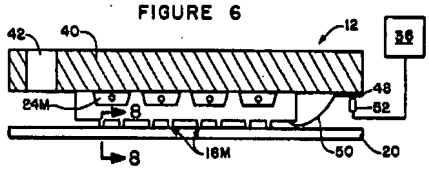

FIGURE 7

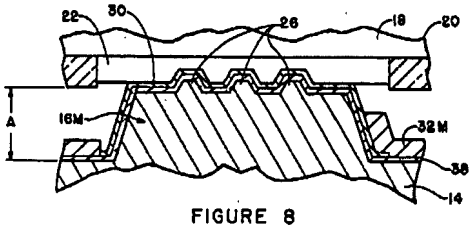

FIGURE 8

as rows of parallel spaced elongated blades. Multiple elongated penetrating projections 26 provide a relatively large surface area for conducting electrical signals to the test pads 22. Although only one penetrating projection 26 is required, with multiple elongated projections 26, current density is spread out and not confined to a small area as can occur with a single pointed or conical member.

(12) The height of each projection 26 is preferably about 1/10 to 3/4 the thickness of the test pads 22 (FIG. 8). The projections 26 will therefore not completely penetrate the full thickness of the test pads 22, as the upper surface 34 (FIG. 3) of the contact members 16 provides a stop plane to limit the penetration depth. In addition, the height of the projections 26 is selected to allow good electrical contact but at the same time to minimally damage the test pads 22. As an example, the height of each projection 26 measured from the surface 34 of the contact member 16 to the tip of the projection 26 can be about 100-10,000 .ANG.. This compares to a representative thickness of the test pads 22 that is typically the same as a metal bond pad on the order of 2,000 to 15,000 .ANG..

(13) Referring to FIGS. 5 and 6, details of the probe card 12 are shown. The probe card 12 includes a test member 10M and a support member 40. The test member 10M is a monolithic structure substantially equivalent to the test member 10 previously described but adapted to simultaneously test four dice 18 at once. As such, the test member 10M includes four patterns of contact members 16M formed superjacent to four etched cavities 24M. Alternately, the test member 10M can be constructed to simultaneously test from one die to all of the dice on a wafer or an integral die multiple (e.g., 8, 16, 32).

(14) In addition, the test member 10M includes a pattern of conductors 32M in electrical communication with the conductive layers for the contact members 16M substantially as previously described. The pattern of conductors 32M can be formed using a metallization process in a desired pattern and with bonding sites on a terminal end thereof.

(15) The test member 10M also includes etched passageways 44 that are in flow communication with the cavities 24M. The etched passageways 44 are also in flow communication with conduits 46 formed of tubing or other suitable material sealingly attached to the test member 10M. The conduits 46 are in flow communication with a fluid or gas supply (not shown) such that a fluid or gas can be injected into the cavities 24M to produce a variable pressure. With this arrangement the flexure of the contact members 16M can be controlled and varied as required.

(16) The test member 10M is sealingly attached to the support member 40

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US006861858B2

(12) **United States Patent**
Chen et al.

(10) **Patent No.: US 6,861,858 B2**
(45) **Date of Patent: Mar. 1, 2005**

(54) **VERTICAL PROBE CARD AND METHOD FOR USING THE SAME**

(75) Inventors: Hsing-Hsin Chen, Taipei Hsien (TW); Howard Hsu, San Jose, CA (US)

(73) Assignee: SCS Hightech, Inc., Taipei Hsien (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 31 days.

(21) Appl. No.: 10/351,096

(22) Filed: Jan. 23, 2003

(65) Prior Publication Data

US 2003/0141889 A1 Jul. 31, 2003

(30) Foreign Application Priority Data

Jan. 24, 2002 (TW) ..... 91101112 A

(51) Int. Cl.[7] G01R 31/02

(52) U.S. Cl. 324/755; 324/761; 324/158.1; 324/754; 257/48

(58) Field of Search 324/755, 765, 324/754, 757, 761, 158.1, 763, 439/482, 700, 71; 257/737, 738; 438/48, 613, 614, 615; 228/180.22; 174/267, 260, 261; 361/722, 773, 774, 783

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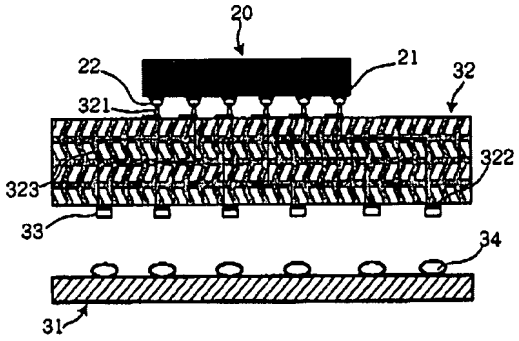
Primary Examiner—Kamand Cuneo
Assistant Examiner—Jimmy Nguyen
(74) *Attorney, Agent, or Firm*—Hogan & Hartson L.L.P.

(57) **ABSTRACT**

A vertical probe card for testing electronic devices includes a multi-layer ceramic substrate mounted on a printed circuit board. The multi-layer ceramic substrate provides a plurality of vertical probes arranged in a planar array and formed on the surface of the multi-layer ceramic substrate by micro-fabrication technology. The method of using the vertical probe card includes disposing a device to be tested under the card, aligning the card's probes with the I/O terminals of the device, and contacting the device with the card's ceramic substrate so that all of the contact portions of the I/O terminals are contacted and deformed by the probes. The relative positions of the electronic device and the apparatus are maintained while Automatic Test Equipment tests the device.

13 Claims, 6 Drawing Sheets



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US-PAT-NO:              6861858
DOCUMENT-IDENTIFIER:    US 6861858 B2
TITLE:                  Vertical probe card and method for using the same
DATE-ISSUED:            March 1, 2005

INVENTOR-INFORMATION:
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Hsu; Howard             San Jose        CA      N/A       N/A

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APPL-NO:    10/351096
DATE FILED: January 23, 2003

FOREIGN-APPL-PRIORITY-DATA:
COUNTRY APPL-NO      APPL-DATE
TW      91101112 A   January 24, 2002

INT-CL-ISSUED:      [07] G01R031/02

INT-CL-CURRENT:
TYPE                IPC DATE
CIPP                G01 R 1/073 20060101

US-CL-ISSUED:       324/755 , 324/761 , 324/158.1 , 324/754 , 257/48

US-CL-CURRENT:      324/755, 257/48 , 324/158.1 , 324/754 , 324/761

FIELD-OF-           324/755; 324/765 ; 324/754 ; 324/757 ; 324/761 ;
CLASSIFICATION-     324/158.1 ; 324/763 ; 439/482 ; 439/700 ; 439/71 ;
SEARCH:             257/737 ; 257/738 ;-438/48 ; 438/613 ; 438/614 ;
                    438/615 ; 228/180.22 ; 174/267 ; 174/260 ; 174/261 ;
                    361/722 ; 361/773 ; 361/774 ; 361/783

**See application file for complete search history**
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US005172050A

United States Patent [19]

Swapp

[11] Patent Number: 5,172,050

[45] Date of Patent: Dec. 15, 1992

[54] MICROMACHINED SEMICONDUCTOR PROBE CARD

[75] Inventor: Marvin Swapp, Mesa, Ariz.

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 655,705

[22] Filed: Feb. 15, 1991

[51] Int. Cl.[5] G01R 1/02; B44C 1/22

[52] U.S. Cl. ..... 324/158 P; 324/72.5; 439/482; 156/653

[58] Field of Search ..... 324/158 P, 158 R, 324/72.5; 439/482; 437/8; 29/852, 825, 846, 842, 843, 827; 156/644, 651, 652, 653, 654, 655

[56] References Cited

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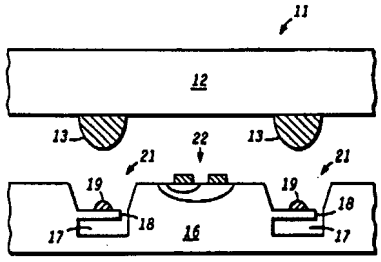
Primary Examiner—Vinh Nguyen

Attorney, Agent, or Firm—Stuart T. Langley

[57] ABSTRACT

A semiconductor probe card having a plurality of micromachined probes tips for contacting an array of electrode pads formed on a semiconductor integrated circuit is provided. The plurality of probe tips are formed on the top surface of the substrate wherein the probe tips are arranged in an array matching of electrode pads on the integrated circuit to be tested. A portion of the semiconductor substrate underneath the probe tips is thin, so that the probe tips rests on a flexible diaphragm or beam.

16 Claims, 2 Drawing Sheets



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US-PAT-NO: 5172050

DOCUMENT-IDENTIFIER: US 5172050 A

See image for Certificate of Correction

TITLE: Micromachined semiconductor probe card

TITLE - TI (1):

Micromachined semiconductor probe card

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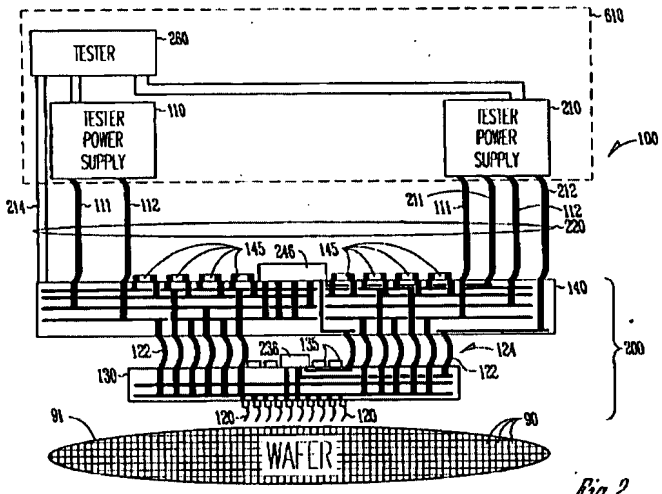

Fig.2

US-PAT-NO: 6897666
DOCUMENT-IDENTIFIER: US 6897666 B2
See image for Certificate of Correction
TITLE: Embedded voltage regulator and active transient control device in probe head for improved power delivery and method
DATE-ISSUED: May 24, 2005

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
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Pan; Jin	Portland	OR	N/A	N/A
Zhu; Hua	San Jose	CA	N/A	N/A
Ding; Jun	Portland	OR	N/A	N/A

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Intel Corporation	Santa Clara	CA	N/A	N/A	02
Primarion, Inc.	Tempe	AZ	N/A	N/A	02

APPL-NO: 10/335195
DATE FILED: December 31, 2002

INT-CL-ISSUED: [07] G01R031/26

INT-CL-CURRENT:

TYPE	IPC DATE
CIPP	G01 R 1/073 20060101

US-CL-ISSUED: 324/754 , 324/765

US-CL-CURRENT: 324/754, 324/765

FIELD-OF-CLASSIFICATION-SEARCH: 324/765; 324/754 ; 324/158.1 ; 324/761 ; 324/757 ; 324/762
See application file for complete search history

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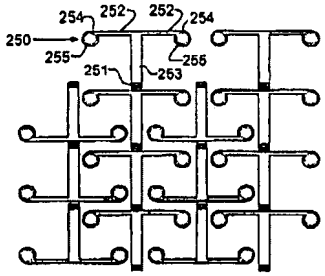

FIG. 17B

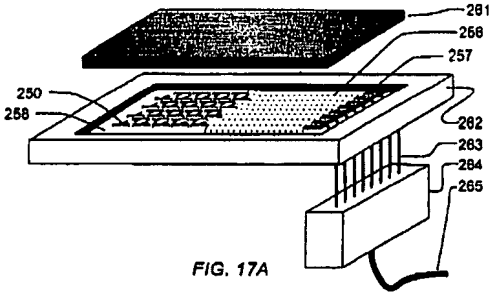

FIG. 17A

(36) FIG. 15B shows a portion of the probes that are disposed on the surface of connector 230. The probe tips are arranged in an area array that is matched to an area array of contact pads on flip-chips being tested. Each probe tip 241 is positioned to mate with a corresponding contact pad on the flip-chip. The dimensions of probe 232 are compatible with a grid pitch spacing of between 150 microns and 500 microns currently utilized for flip-chips. Probes 232 are arranged in a nested pattern that allows each probe to fit the space available. In a preferred embodiment, additional non-functional probes are added to the array to provide support to the wafer under test in local regions where the average density of contact pads on the wafer is low. Any required dimensions are suitable for the invention.

(37) Probe tips 241 of probe 232 provide a hard surface for the purpose of breaking through any oxide on the aluminum bond pads on the wafer under test. Probe tip 241 is disposed at the apex of a "V" shaped elongated thin sheet 242 that is supported by posts 245 joined to contact pads 244 at each end of sheet 242.

(38) Compliant probes according to the teachings of this invention provide a means to test high-speed integrated circuits because of the low self and mutual inductance of each probe. A probe card 249 incorporating compliant probes is shown in FIG. 16A. Probes 240 are disposed in an area array pattern on a substrate 248 suitable for testing flip-chips with area array contact pads. Each probe 240 is connected electrically to terminals 247 on probe card 249 by circuit trace means 246 incorporated in substrate 248. Substrate 248 is preferably made of a dimensionally stable base such as alumina ceramic material, on which circuit traces are disposed between layers of polyimide dielectric material.

(39) FIG. 16B shows an array of compliant probes 240 configured according to the teachings of the invention illustrated in FIG. 5, for example. A probe tip 241 is disposed at the end of extension arm 243 at the midpoint of elongated sheet spring 242. Support posts 244 are joined to contact pads 245 at each end of elongated sheet spring 242 so that probe tip 241 on arm 243 is moveably compliant in a vertical direction.

(40) A chip socket shown in FIG. 17A provides a demountable means for testing, burning-in and operating flip-chips. Flip-chip 261 is held by positioning means 262 such that each contact pad on flip-chip 261 is mated with a corresponding probe 250 on the surface of socket substrate 258. Each probe 250 is connected electrically with terminals 257 on socket substrate 258 by circuit trace means 256. Electrical signals suitable for operating flip-chip 261 are directed to the socket by interconnection means 263 from electronic circuitry means 264. Cable 265 connects the

Probe card - chip socket of 17A

~~Substrate - 258~~

probe - 250, 258

Turtel - Fig. 17A (inherent)

Ref. B